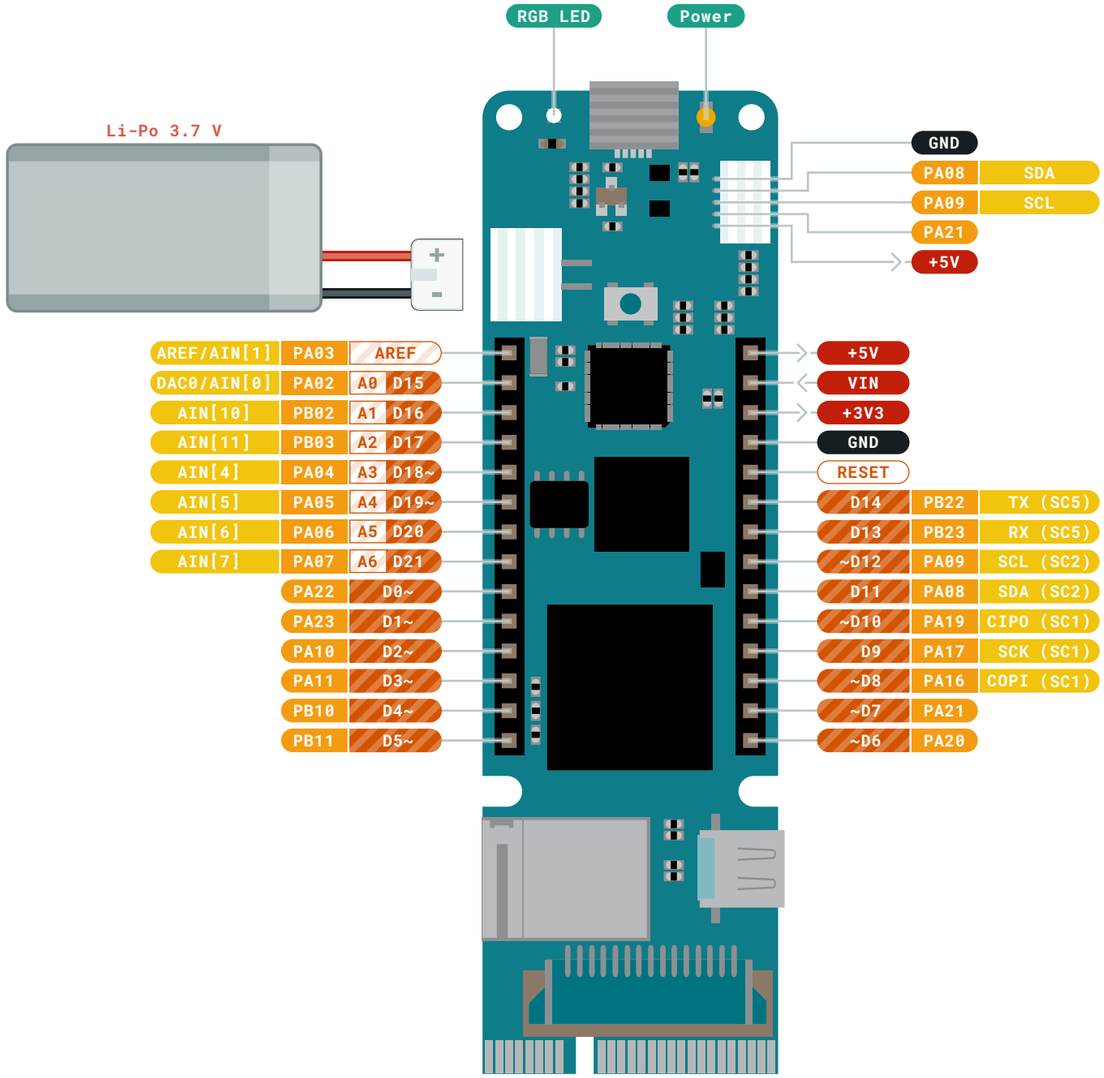
ARDUINO

ARDUINO
MKR VIDOR 4000

STORE.ARDUINO.CC/MKR-VIDOR-4000



- Ground
- Power
- LED
- Internal Pin
- SWD Pin
- Digital Pin
- Analog Pin
- Other Pin
- Microcontroller's Port
- Default
- FPGA Port

If programmed with SAMD

- **MAXIMUM** current per pin is 7mA
- **MAXIMUM** source current is 46mA
- **MAXIMUM** sink current is 65mA per pin group

If programmed with FPGA

- **MAXIMUM** current if the I/O standard configuration 3.3-V LVTTL is 4mA
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVCMOS is 2mA

VIN Input voltage to the board.

NOTE: CIPO/COPI have previously been referred to as MISO/MOSI

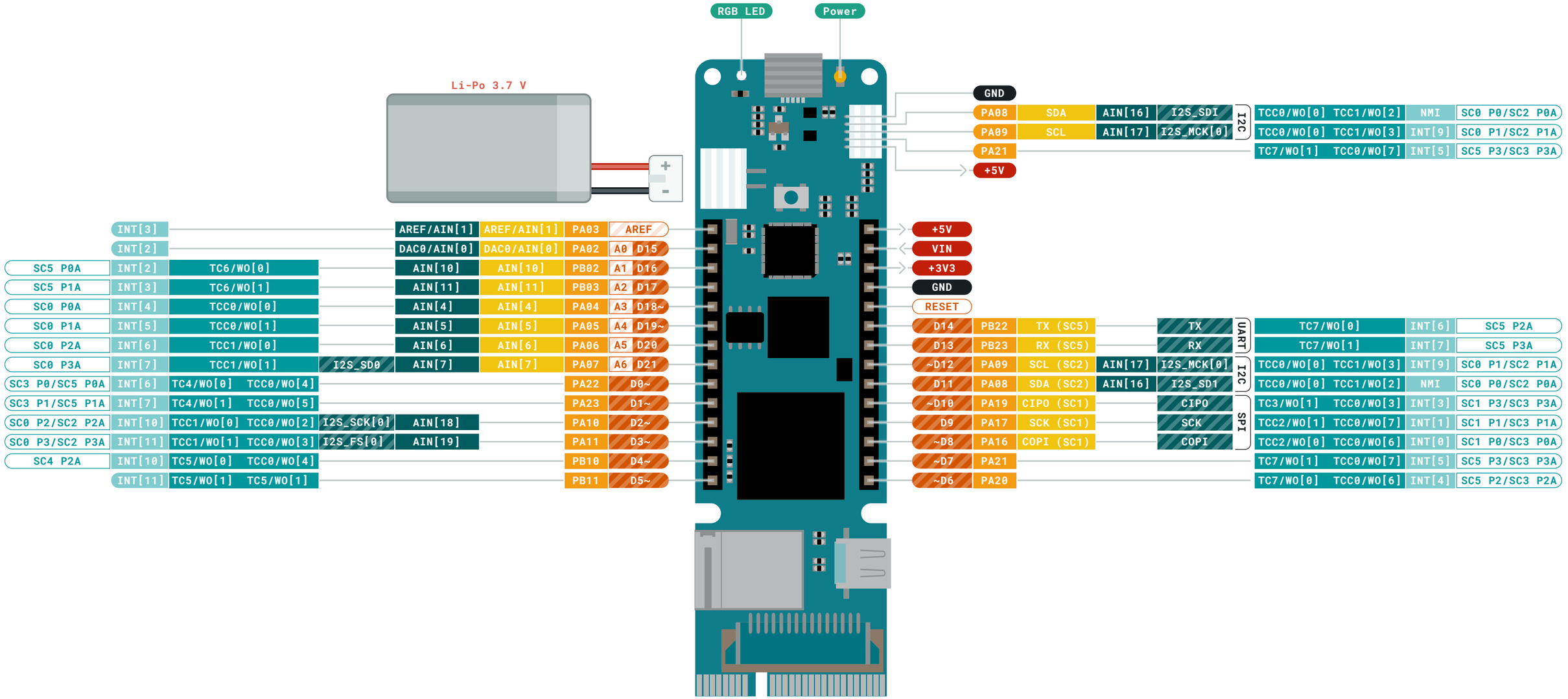
ARDUINO.CC

Last update: 4/08/2020

ARDUINO

ARDUINO
MKR VIDOR 4000

STORE.ARDUINO.CC/MKR-VIDOR-4000



- Ground
- Power
- LED
- Internal Pin
- SWD Pin
- Digital Pin
- Analog Pin
- Other Pin
- Microcontroller's Port
- Default
- FPGA Port
- Analog
- Communication
- Timer
- Interrupt
- Sercom

If programmed with SAMD

- **MAXIMUM** current per pin is 7mA
- **MAXIMUM** source current is 46mA
- **MAXIMUM** sink current is 65mA per pin group

If programmed with FPGA

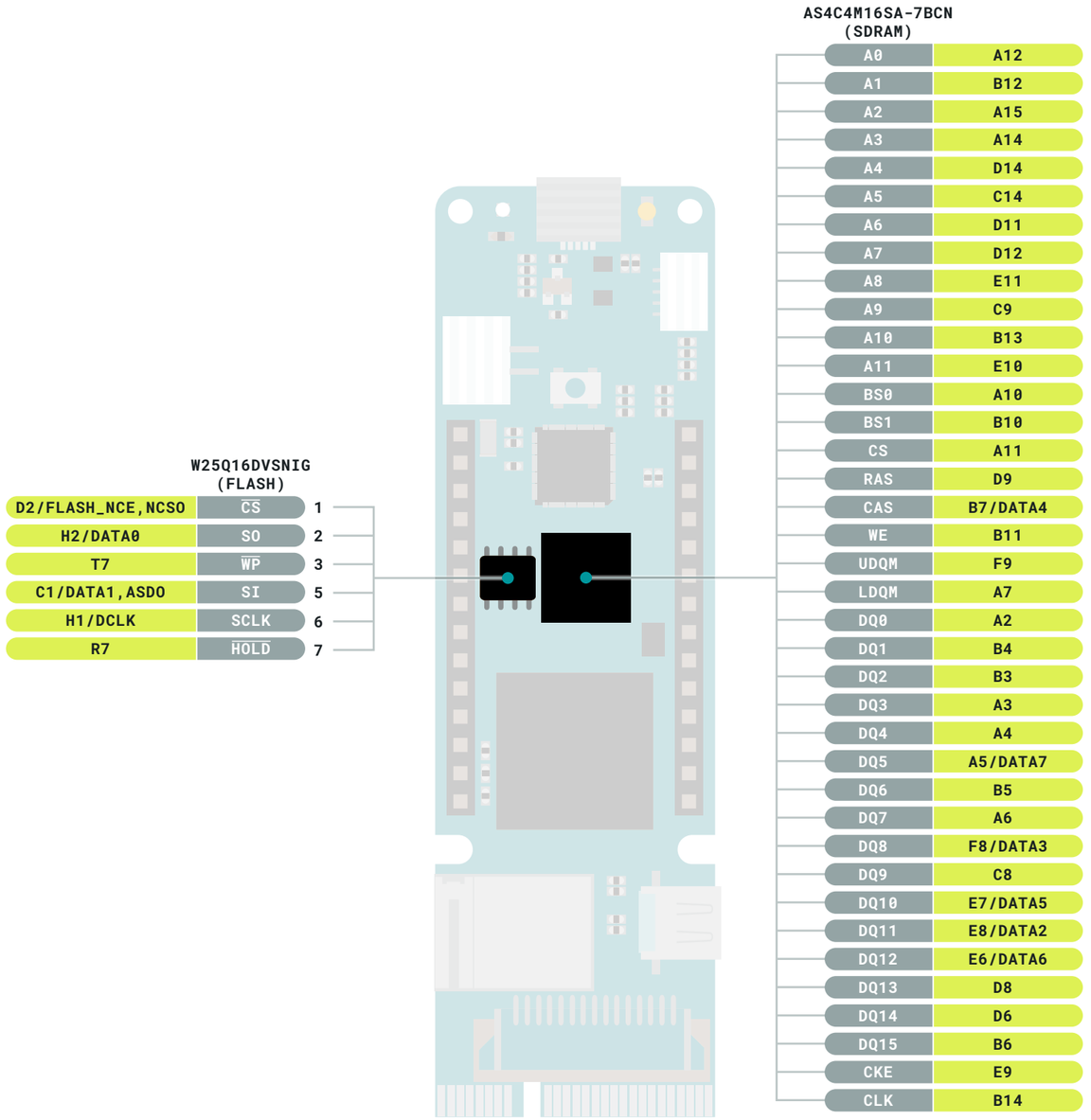
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVTTL is 4mA
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVCMOS is 2mA

VIN Input voltage to the board.

NOTE: CIPO/COPI have previously been referred to as MISO/MOSI

ARDUINO.CC

Last update: 4/08/2020



- Ground
- Power
- LED
- Internal Pin
- SWD Pin
- Digital Pin
- Analog Pin
- Other Pin
- Microcontroller's Port
- Default
- FPGA Port

If programmed with SAMD

- **MAXIMUM** current per pin is 7mA
- **MAXIMUM** source current is 46mA
- **MAXIMUM** sink current is 65mA per pin group

If programmed with FPGA

- **MAXIMUM** current if the I/O standard configuration 3.3-V LVTTL is 4mA
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVCMOS is 2mA

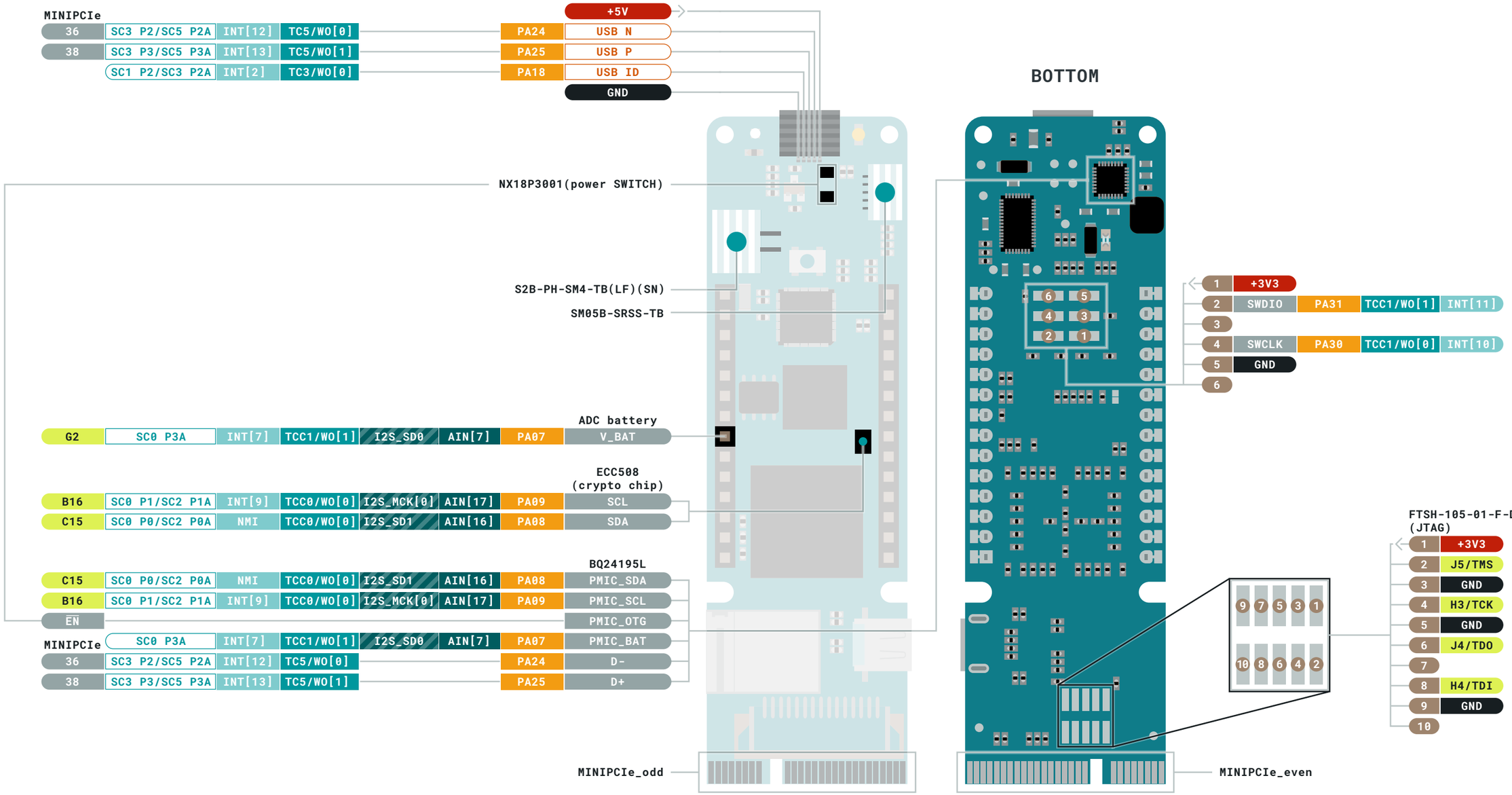
VIN Input voltage to the board.

ARDUINO.CC

Last update: 4/08/2020

ARDUINO
MKR VIDOR 4000

STORE.ARDUINO.CC/MKR-VIDOR-4000



- Ground
- Power
- LED
- Internal Pin
- SWD Pin
- Digital Pin
- Analog Pin
- Other Pin
- Microcontroller's Port
- Default
- FPGA Port
- Analog
- Communication
- Timer
- Interrupt
- Sercom

If programmed with SAMD

- **MAXIMUM** current per pin is 7mA
- **MAXIMUM** source current is 46mA
- **MAXIMUM** sink current is 65mA per pin group

If programmed with FPGA

- **MAXIMUM** current if the I/O standard configuration 3.3-V LVTTL is 4mA
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVCMOS is 2mA

VIN Input voltage to the board.

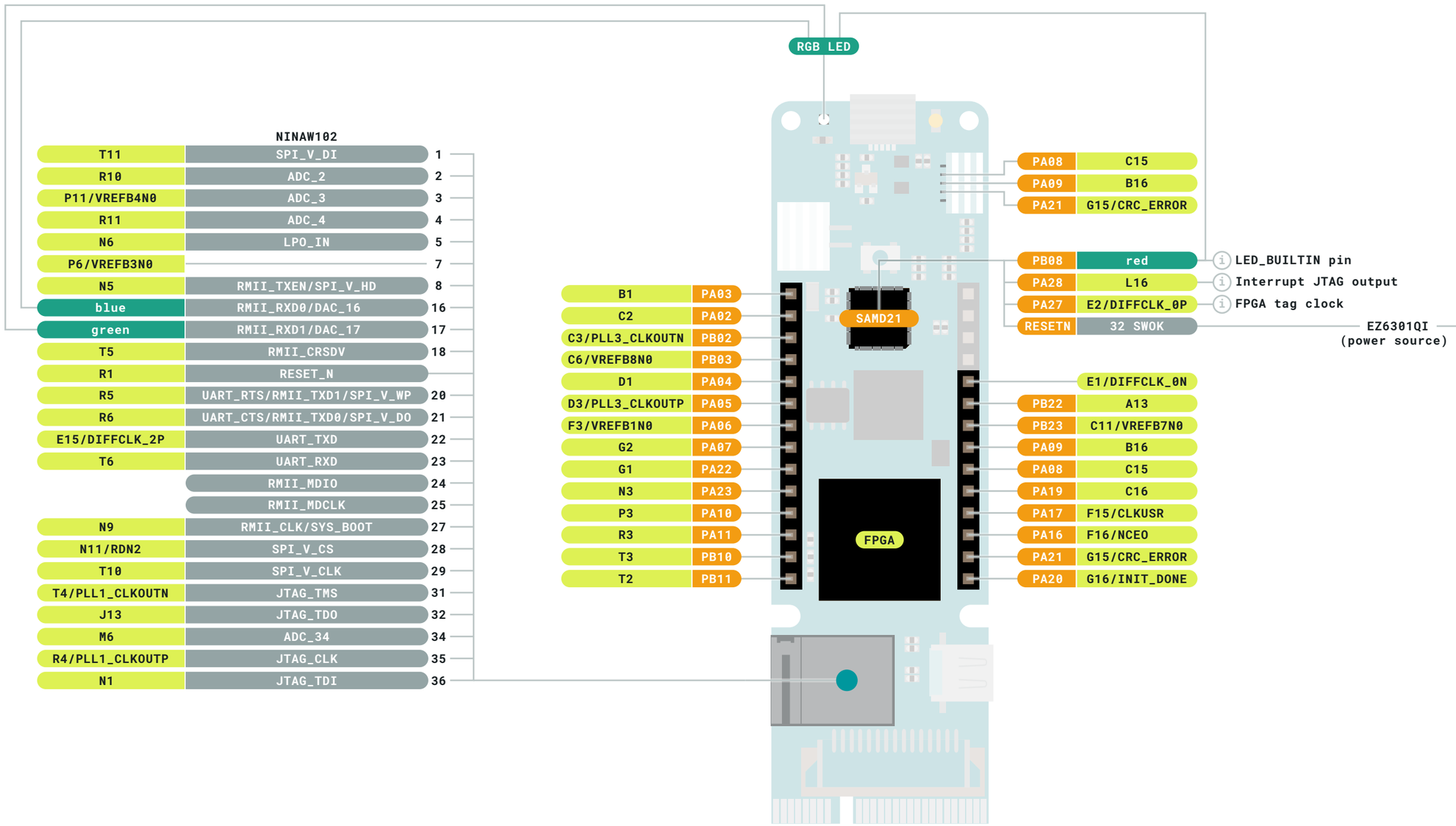
ARDUINO.CC

Last update: 4/08/2020

ARDUINO

ARDUINO
MKR VIDOR 4000

STORE.ARDUINO.CC/MKR-VIDOR-4000



- Ground
- Power
- LED
- Internal Pin
- SWD Pin
- Digital Pin
- Analog Pin
- Other Pin
- Microcontroller's Port
- Default
- FPGA Port

If programmed with SAMD

- **MAXIMUM** current per pin is 7mA
- **MAXIMUM** source current is 46mA
- **MAXIMUM** sink current is 65mA per pin group

If programmed with FPGA

- **MAXIMUM** current if the I/O standard configuration 3.3-V LVTTL is 4mA
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVCMOS is 2mA

VIN Input voltage to the board.

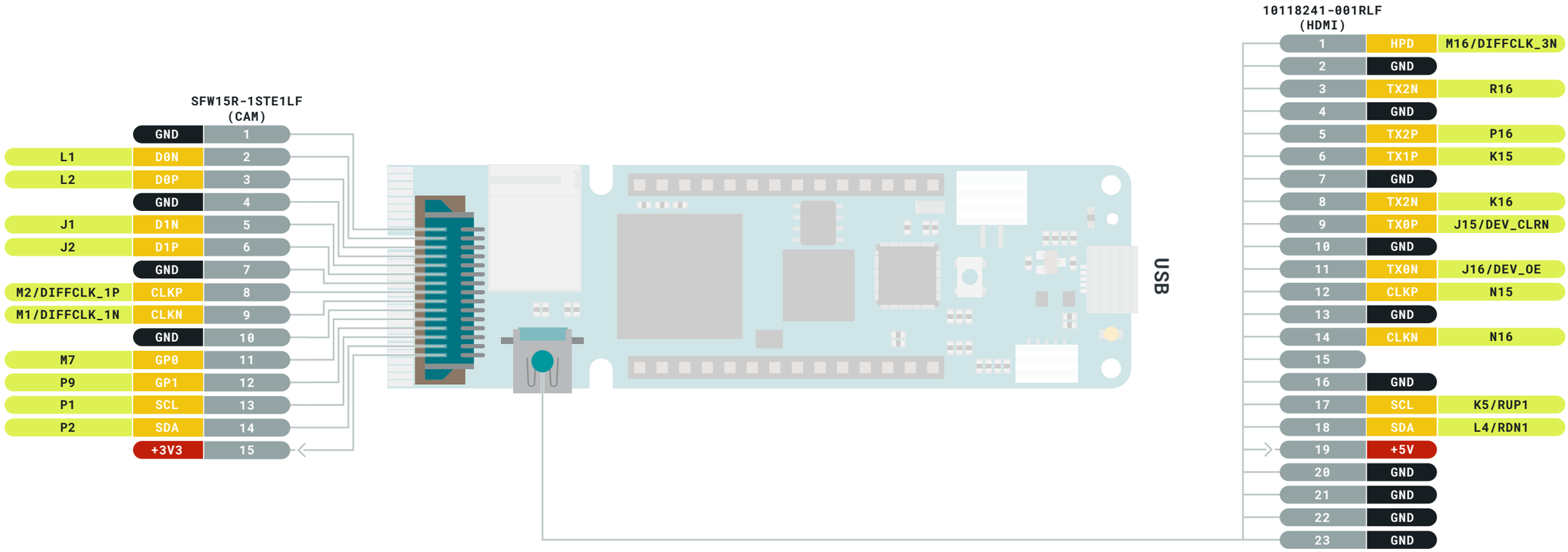
ARDUINO.CC

Last update: 4/08/2020

ARDUINO

ARDUINO
MKR VIDOR 4000

STORE.ARDUINO.CC/MKR-VIDOR-4000



Ground
Power
LED
Internal Pin
SWD Pin

Digital Pin
Analog Pin
Other Pin
Microcontroller's Port
Default
FPGA Port

If programmed with SAMD

- **MAXIMUM** current per pin is 7mA
- **MAXIMUM** source current is 46mA
- **MAXIMUM** sink current is 65mA per pin group

If programmed with FPGA

- **MAXIMUM** current if the I/O standard configuration 3.3-V LVTTL is 4mA
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVCMOS is 2mA

VIN Input voltage to the board.

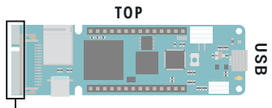
ARDUINO.CC

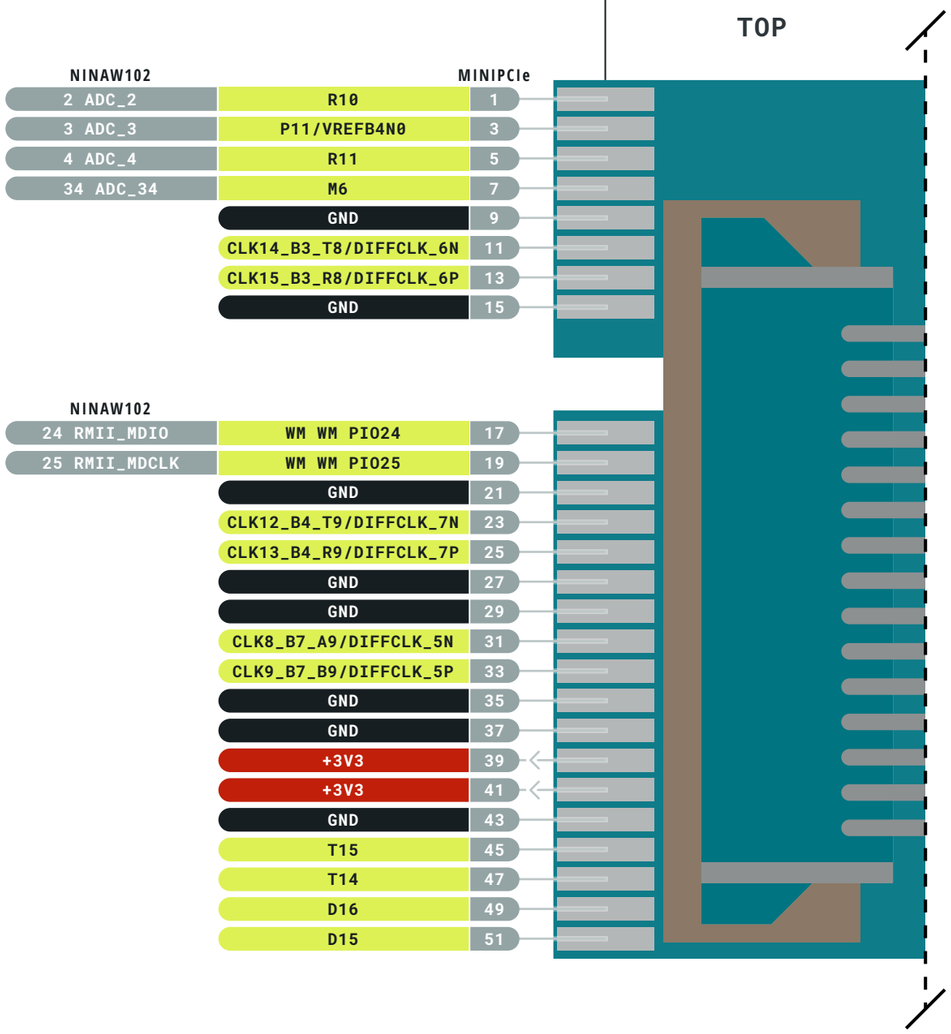
Last update: 4/08/2020

ARDUINO MKR VIDOR 4000

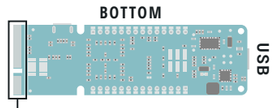
STORE.ARDUINO.CC/MKR-VIDOR-4000

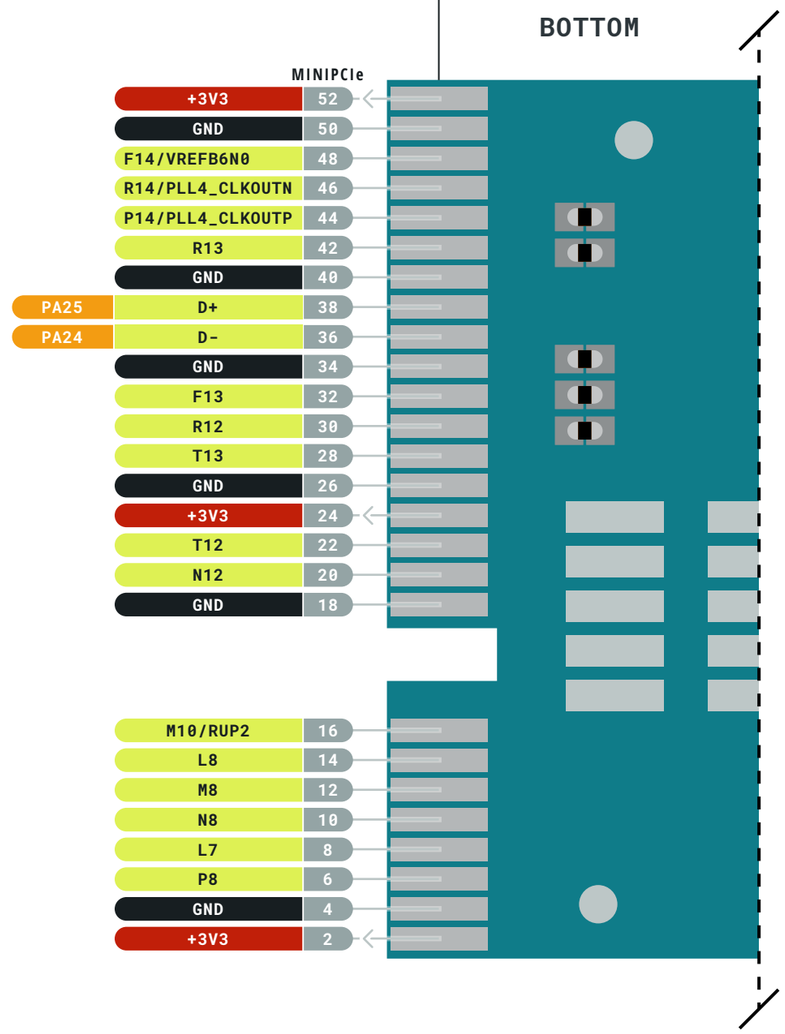
MINIPCIe_odd





MINIPCIe_even





- Ground
- Power
- LED
- Internal Pin
- SWD Pin
- Digital Pin
- Analog Pin
- Other Pin
- Microcontroller's Port
- Default
- FPGA Port

If programmed with SAMD

- **MAXIMUM** current per pin is 7mA
- **MAXIMUM** source current is 46mA
- **MAXIMUM** sink current is 65mA per pin group

If programmed with FPGA

- **MAXIMUM** current if the I/O standard configuration 3.3-V LVTTL is 4mA
- **MAXIMUM** current if the I/O standard configuration 3.3-V LVCMOS is 2mA

VIN Input voltage to the board.

ARDUINO.CC

Last update: 4/08/2020